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 approach can provide
 the three-dimensional
 computational tool
 necessary to handle
 the geometric and
 material complexities
 of real semiconductor
 devices. The
 dimensions of an
 electrically active
 region (e.g., gate) are
 typically in fractions of
 a micrometer while the
 thickness of circuit
 topology features (e.g.,
 lines, metallization,
 pads) can vary from a
 few tens to a few
 thousands of
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