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(10 Gates) With A MUX (4 Gates), As
Shown In Figure 1. Suppose That Your
Chip (non-scan Design) Has 120,000
Logic Gates And 2,200 D Flip-flops. A
Combinational ATPG Program Produced
600 Vectors To Fully Test The Logic.

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Here on this page, you will find the Latest Wipro Placement Questions with similar patterns which we have analyzed from Previous Year Wipro placement

papers with solutions for 2020 are discussed below. As seen from Wipro's previous papers the test is of moderate difficulty.

Wipro Placement Papers 2020 and Questions with Answers ...

1) Explain how logical gates are controlled by Boolean logic? In Boolean algebra, the true state is denoted by the number one, referred as logic one or logic high. While, the false state is represented by the number zero, called logic zero or logic low. And in the digital electronic, the logic high is denoted by the presence of a voltage potential.

Top 17 VLSI Interview Questions & Answers

Qualcomm Written Test Overview. Qualcomm had changed its curriculum in May 2019. Here you can find the test pattern of Qualcomm Placement paper. In Qualcomm, there is 0.25 negative marking in the Qualcomm placement paper. Qualcomm Placement Papers have the following sections in the exam - Total Number of Questions - 60 Questions; Total Time ...

Qualcomm Placement Papers and Previous Papers Questions ...

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